文件编号：QFN_Addendum
修订版 0，2014 年 7 月

新的 QFN 软件包迁移的附录

本增编提供了本书所涵盖产品的98A案例大纲编号的更改。由于一些包裹从金线迁移到铜线，案例大纲发生了变化。有关旧（金线）包装与新（铜线）包装，请参阅下表。

要查看新绘图，请访问 Freescale.com 并搜索您设备的新 98A 软件包编号。

有关 QFN 软件包使用的更多信息，请参阅 EB806： *QFN 和 DFN 封装上裸露垫的电气连接建议*。

部件号	包裹描述	原始（金丝）包裹文件编号	当前（铜线）包装文件号
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

新的 QFN 软件包迁移的附录，Rev. 0

特点

- 8 位 HCS08 中央处理器单元（CPU）

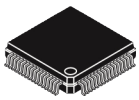
- 高达 20MHz 的 CPU，温度范围为-40°C 至 85°C，温度范围为 3.6V 至 1.8V
- 添加了 BGND 指令的 HC08 指令集
- 支持多达 32 个中断/重置源

- 片上存储器
  - 双阵列 FLASH 读取/编程/擦除全工作电压和温度
  - 随机存取存储器（RAM）
  - 防止未经授权访问 RAM 和 FLASH 内容的安全电路
- 省电模式
  - 两种低功耗停止模式
  - 减电等待模式
  - 低功耗运行和等待模式允许外围设备在稳压器处于待机状态时运行
  - 外围时钟门控寄存器可以禁用未使用模块的时钟，从而减少电流。
  - 非常低功率的外部振荡器，可用于 stop2 或 stop3 模式，为实时计数器提供准确的时钟源
  - 6 使用从停止 3 模式的典型唤醒时间
- 时钟源选项
  - 振荡器（XOSC）——环控穿孔振荡器；晶体或陶瓷谐振器范围为 31.25 kHz 至 38.4 kHz 或 1 MHz 至 16 MHz
  - 内部时钟源（ICS）——包含由内部或外部参考控制的频率锁定环（FLL）的内部时钟源模块；内部参考的精确修剪允许 0.2%的分辨率和 2%的温度和电压偏差；支持 1MHz 至 10 MHz 的总线频率。
- 系统保护
  - 看门狗计算机正常运行（COP）重置
    可以选择从专用的 1kHz 内部时钟源运行或

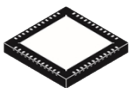
    公交车时钟
  - 带中断的低电压警告
  - 带重置或中断的低电压检测
  - 带有重置的非法操作码和非法地址检测
  - 闪光块保护

- 发展支持
  - 单线后台调试接口
  - 断点功能允许在电路调试期间设置单个断点（加上片上调试模块中的另外两个断点）

文件编号：MC9S08LL16
2013 年 1 月 7 日修订版


64-LQFP
Case 840F


48-LQFP
Case 932


48-QFN
1314

- 片上电路内模拟器（ICE）调试模块，包含三个比较器和九个触发模式。八个深度 FIFO，用于存储流量更改地址和仅事件数据。调试模块支持标签和强制断点

- 外围设备
  - **液晶显示器**—4x28 或8x24 液晶驱动器，带内部充电泵和提供内部调节的液晶参考选项，可以修剪用于对比度控制。
  - **ADC**— 8 通道，12 位分辨率；2.5 Ms 转换时间；自动比较功能；温度传感器；内部带隙参考通道；在停止 3 中运行；从 3.6V 到 1.8V 全功能
  - **ACMP**—在上升、下降或比较器输出的任何边缘时具有可选中断的模拟比较器；将选项与固定的内部带隙参考电压进行比较；输出可以选择路由到 TPM 模块；在停止时运行 3
  - **科学**—全双工不返回零（NRZ）；LIN 主扩展中断生成；LIN 从扩展中断检测；在活动边缘唤醒
  - **SPI**—全双工或单线双向；
    双缓冲发送和接收；主模式或从模式；
    MSB 优先或 LSB 优先换班
  - **IIC**— IIC 高达 100 kbps，最大总线加载；多主操作；可编程从属地址；中断驱动的字节数据传输；支持广播模式和 10 位寻址
  - **TPMx**—两个 2 通道（TPM1 和TPM2）；每个通道上的可选输入捕获、输出比较或缓冲边缘或中心对齐 PWM；
  - **托德**—（每日时间）带匹配寄存器的 8 位四分之一秒计数器；用于精确时间基数、每日时间、日历或任务调度功能的外部时钟源；免费运行的芯片上低功耗振荡器（1 kHz），用于没有外部组件的循环唤醒。

- 输入/输出
  - 38 个 GPIO，2 个仅输出引脚
  - 8 个具有可选极性的 KBI 中断
  - 所有输入引脚上的滞后和可配置的上拉装置；所有输出引脚上可配置的摆率和驱动强度。

- 套餐选项
  - 64-LQFP、48-LQFP 和 48-QFN

目录

修订历史

为了提供最新信息，我们在万维网上的文件修订将是最新的。您的打印副本可能是更早的修订版。要验证您是否有可用的最新信息，请参阅：

Http://freescale.com/

以下修订历史记录表总结了本文档中包含的更改。

每分钟转速	日期	更改描述
1	2008 年 9 月	初始发布。
2	2008 年 10 月	更新了电气特性。
3	2009 年 1 月	更正了引脚 29、30、32 和 32 英寸的 48 针 QFN/LQFP 引脚 图 3。从供应电流表中提取停止模式加法器，并为数据创建了一个单独的表（请参阅 表 10）。在电源电流特性中添加了缺失的功耗参数（表 9).
4	2009 年 7 月 21 日	已完成所有待定。 更改了 VDDAD 去 V DDA，VSSAD 去 V SSA，我 DDAD 来我 DDA。 更正了数据 表 8，并添加 |我 InT|.完成了图 第 3.6 节“直流特性”.” 更正的 RI 女儿在 FEI 模式下，所有模块都打开，WI 女儿在 8 MHz，所有模块关闭的 FEI 模式，S2I 女儿，S3I 女儿；添加了 ApS3I 女儿在 表 9. 更正的 E 星期二，DNL，INL，EZS，EFS，E 问，和 EIL 在 表 18.
5	2009 年 10 月 13 日	更新的 RPU/R 付讫数据在 表 8。额外的 图 5.

6	2010 年 10 月 27 日	更改了 R 的 Max。PU/R 付讫在 PTA[4:5]，PTD[0:77]和 PTE[0:7]至 69.5 KΩ 在 表 8.
7	2013 年 1 月 23 日	更新 |我锢|在 表 8.

相关文档

查找所有文档的最新版本：http://www.freescale.com

参考手册　　（MC9S08LL16RM）

包含广泛的产品信息，包括操作模式、内存、重置和中断、寄存器定义、端口引脚、CPU 和所有模块信息。

1　MC9S08LL16 系列中的设备

表 1 总结了 MC9S08LL16 系列 MCU 中可用的功能集。

表 1。MCU 和封装的 MC9S08LL16 系列功能

特征	MC9S08LL16		MC9S08LL8
包裹	64 针 LQFP	48 针 QFN/LQFP	48 针 QFN/LQFP
闪光灯	16,384（双 8K 阵列）		10240（8K 和 2K 阵列）
公羊	2080	2080	2080
ACMP	是	是	是
ADC	8ch	8ch	8ch
IIC	是	是	是
IRQ	是	是	是
KBI	8	8	8
科学	是	是	是
SPI	是	是	是
TPM1	2ch	2ch	2ch
TPM2	2ch	-	-
托德	是	是	是
液晶显示器	8x24 4x28	8x16 4x20	8x16 4x20

I/O 引脚 [1]	38	31	31

[1] I/O does not include two output-only port pins.

The block diagram in Figure 1 shows the structure of the MC9S08LL16 series MCU.

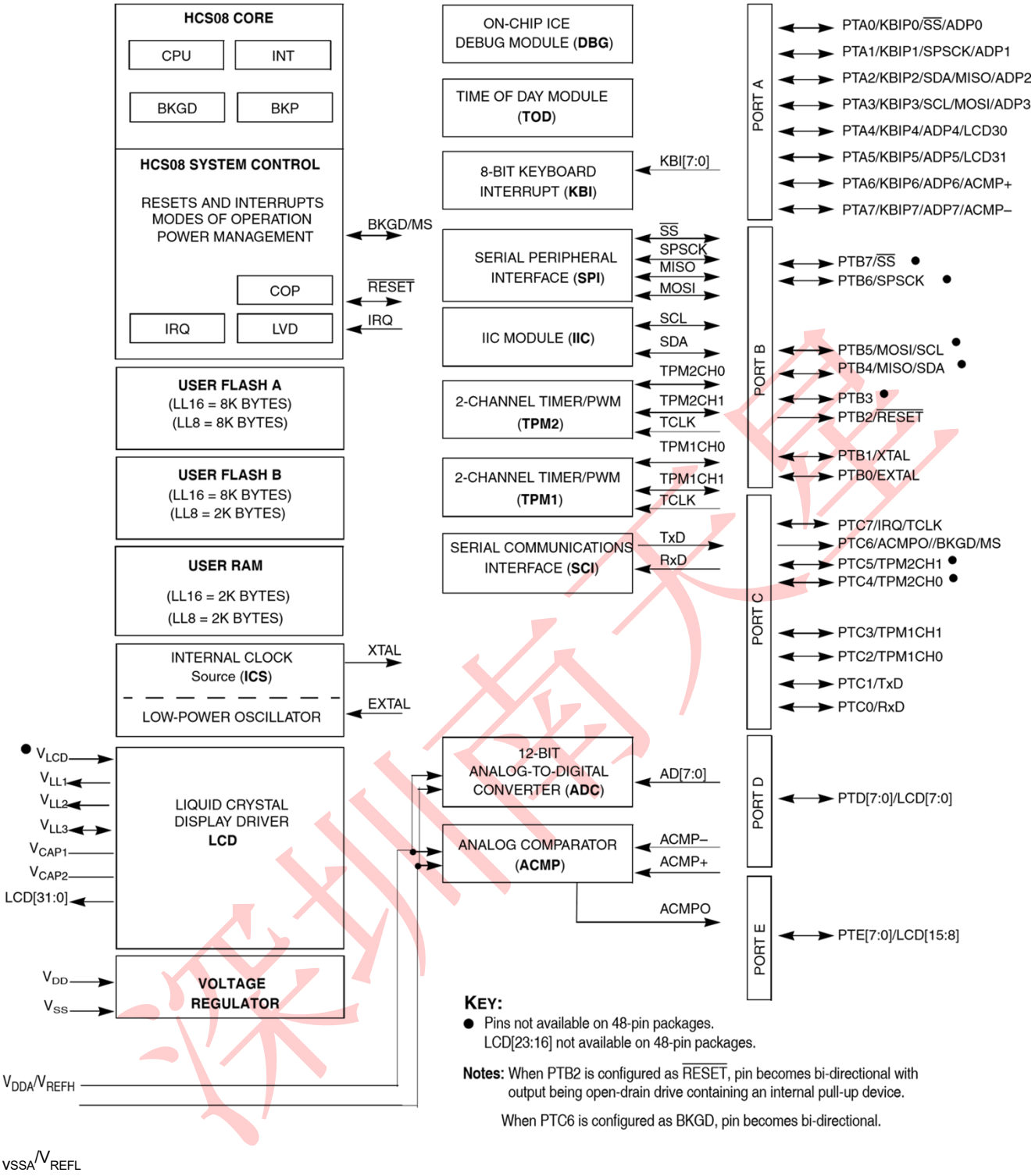
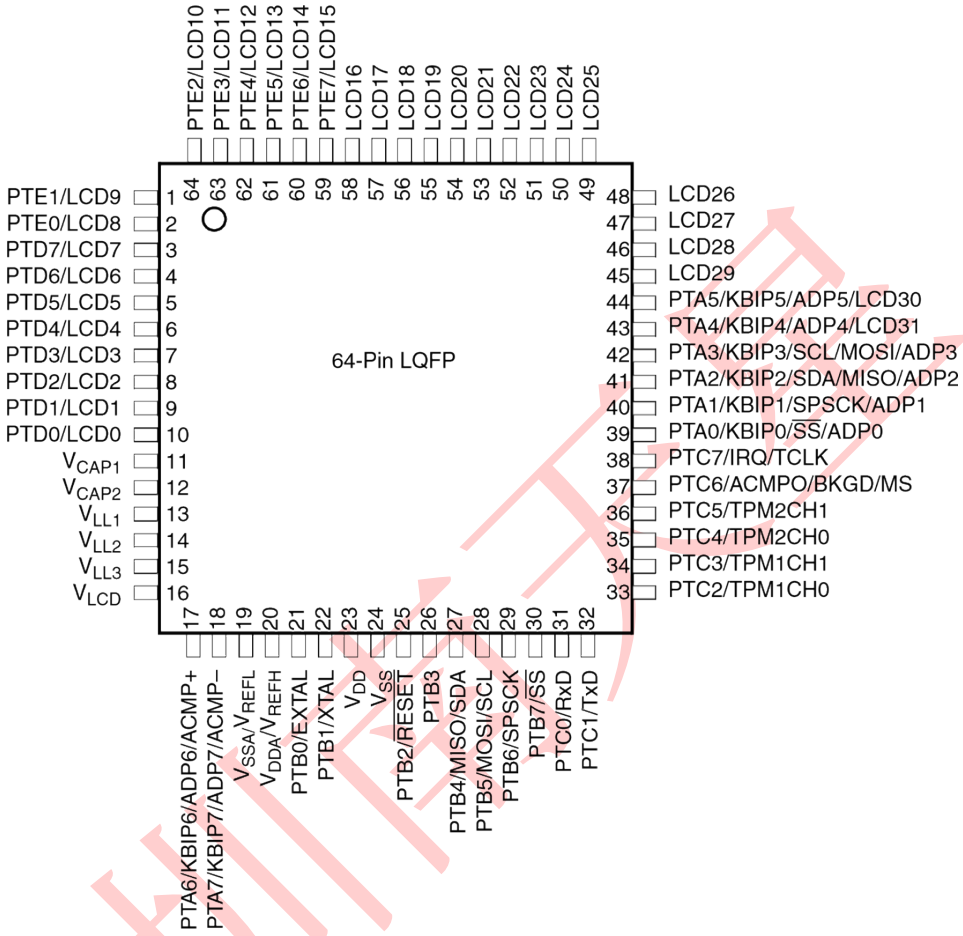


图 1。MC9S08LL16 系列方框图

引脚分配

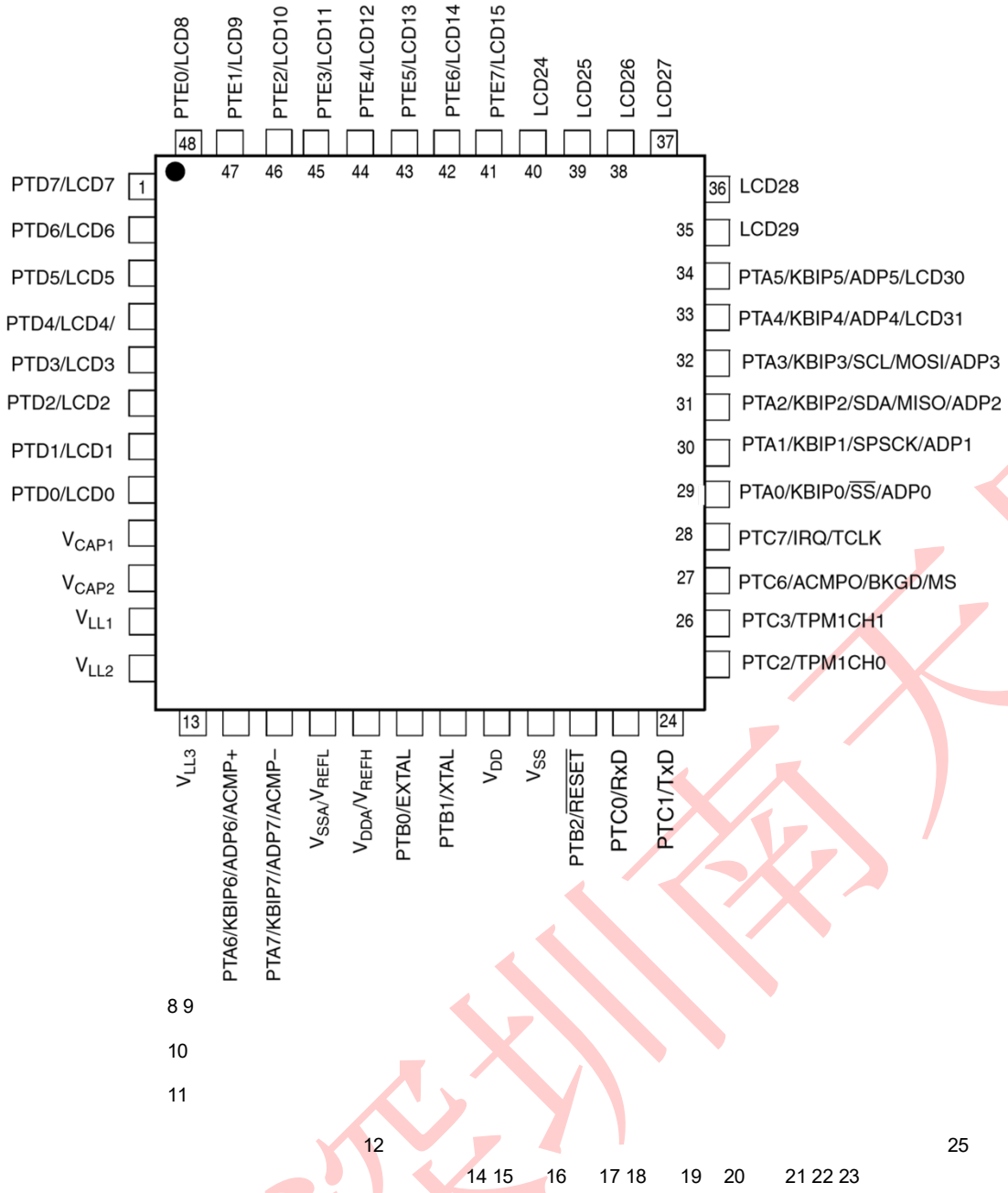
2 引脚分配

本节显示 MC9S08LL16 系列设备的引脚分配。



注：V_{REFH}/V_{REFL} 内部连接到 V_{DDA}/V_{SSA}.

图 2。64 针 LQFP 封装的 MC9S08LL16 系列引脚分配



48 针 QFN/LQFP

注：V_{REFH}/V_{REFL} 内部连接到 V_{DDA}/V_{SSA}

图 3。48 针 QFN/LQFP 封装中的 MC9S08LL16 系列

引脚分配

表 2。按包引脚计数的引脚可用性

		<--最低 **优先地位** -->最高				
64	**48**	**端口销**	**Alt 1**	**替代 2**	**Alt3**	**Alt4**
1	47	PTE1	LCD9			
2	48	PTE0	液晶显示器 8			
3	1	PTD7	液晶 7			
4	2	PTD6	LCD6			
5	3	PTD5	液晶显示器 5			
6	4	PTD4	液晶显示器 4			
7	5	PTD3	液晶 3			
8	6	PTD2	液晶显示器 2			
9	7	PTD1	LCD1			
10	8	PTD0	液晶屏 0			
11	9		V 帽子 1			
12	10		V 上限 2			
13	11		VLL1			
14	12		VLL2			
15	13		VLL3			
16	—		V 液晶显示器			
17	14	PTA6	KBIP6	ADP6	ACMP+	
18	15	PTA7	KBIP7	ADP7	ACMP-	
19	16				VSSA	
					VREFL	

20	17				VREFH	
					VDDA	
21	18	PTB0		EXTAL		
22	19	PTB1		XTAL		
23	20				V 女儿	
24	21				V 纳粹党卫军	
25	22	PTB2	调整			
26	—	PTB3				
27	—	PTB4	—	米索	SDA	
28	—	PTB5	—	莫西	SCL	
29	—	PTB6	—	SPSCK		
30	—	PTB7	—	纳粹党卫军		
31	23	PTC0		RxD		
32	24	PTC1		TxD		
33	25	PTC2		TPM1CH0		
34	26	PTC3		TPM1CH1		
35	—	PTC4		TPM2CH0		
36	—	PTC5		TPM2CH1		
37	27	PTC6	ACMPO	BKGD	女士	
38	28	PTC7		IRQ	TCLK	
39	29	PTA0	KBIP0	—	纳粹党卫军	ADP0

表 2。按包引脚计数的引脚可用性（续）

		<--最低 优先地位 -->最高				
64	**48**	**端口销**	**Alt 1**	**替代 2**	**Alt3**	**Alt4**
40	30	PTA1	KBIP1	—	SPSCK	ADP1
41	31	PTA2	KBIP2	SDA	米索	ADP2
42	32	PTA3	KBIP3	SCL	莫西	ADP3
43	33	PTA4	KBIP4	ADP4	液晶屏 31	
44	34	PTA5	KBIP5	ADP5	LCD30	
45	35		液晶 29			
46	36		LCD28			
47	37		LCD27			
48	38		液晶显示器 26			
49	39		液晶显示器 25			
50	40		LCD24			
51	—		LCD23			
52	—		LCD22			
53	—		LCD21			
54	—		液晶 20			
55			LCD19			
56			液晶显示器 18			
57			LCD17			
58			液晶显示器 16			
59	41	PTE7	LCD15			
60	42	PTE6	液晶显示器 14			
61	43	PTE5	液晶显示器 13			

62	44	PTE4	液晶 12			
63	45	PTE3	液晶显示器 11			
64	46	PTE2	液晶 10			

3 电气特性

3.1 简单介绍

本节包含发布时可用的 MC9S08LL16 系列微控制器的电气和定时规格。

3.2 参数分类

本补编中显示的电气参数由各种方法保证。为了使客户更好地了解，使用以下分类，并酌情在表格中相应标记参数：

表 3。参数分类

P	在每个设备的生产测试期间，这些参数是有保证的。
字母 C	这些参数是通过测量跨过程变化的统计相关样本大小的设计表征来实现的。
字母 T	除非另有说明，否则这些参数是通过在典型条件下从典型设备对小样本尺寸进行设计表征来实现的。典型列中显示的所有值都属于此类别。
d	这些参数主要来自模拟。

笔记

分类酌情显示在参数表中标有“C”的列中。

3.3 绝对最高评级

绝对最大额定值仅为应力额定值，不能保证最大值的功能运行。压力超过规定的极限 表 4 可能影响设备可靠性或对设备造成永久性损坏。有关功能操作条件，请参阅本节中的其余表格。

该设备包含防止高静态电压或电场造成的损坏的电路；但是，建议采取正常的预防措施，以避免将任何高于最大额定电压的电压应用于此高阻抗电路。如果未使用的输入与适当的逻辑电压电平绑定，操作的可靠性会提高（例如，要么 $V_{纳粹党卫军}$ 或 $V_{女儿}$）或启用与引脚关联的可编程上拉电阻。

表 4。绝对最高评级

评分	标志	价值	单位
电源电压	$V_{女儿}$	–0.3 到 3.8	V

最大电流进入 V 女儿	我女儿	120	妈
数字输入电压	V 锢	–0.3 到 V 女儿+ 0.3	V
瞬时最大电流 单针限制（适用于所有端口针脚）[23，2，4]	我 d	±25	妈
存储温度范围	字母 Tstg	–55 到 150	°字母 C

3.4 热特性

本节提供有关工作温度范围、功耗和包装热阻的信息。与片上逻辑和电压调节器电路中的功耗相比，I/O 引脚上的功耗通常很小，并且由用户决定，而不是由 MCU 设计控制。拿 $P_{I/O}$ 在功率计算中，确定实际引脚电压和V 之间的差异 纳粹党卫军或 V 女儿并乘以每个 I/O 引脚的引脚电流。除了异常高的引脚电流（重载荷）外，引脚电压和 V 之间的差异 纳粹党卫军或 V 女儿会很小。

表 5。热特性

评分	标志	价值	单位
工作温度范围 （包装）	字母 T 罗 马 字母的第一个 字母	字母 T 字母I去 T h – 40到 85	°字母 C
最大结点温度	字母 TJM	95	°字母 C
耐热性 单层板			
64 针 LQFP	ΘJA	72	°C/W
48 针 QFN		84	
48 针 LQFP		81	
热阻 四层板			
64 针 LQFP	ΘJA	54	°C/W

[2] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[3] All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

[4] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

48 针 QFN		30	
48 针 LQFP		57	

平均芯片结温度（T 第十个英文字母 J）在 °C 可以从以下地址获得：

$$字母\ T_{第十个英文字母\ J} = T_{罗马字母的第一个字母} + (P_d \times \Theta_{JA}) \quad \textit{Eqn。3-1}$$

在哪里：

字母 T 罗马字母的第一个字母 =环境温度， °字母 C

Θ_{JA}= 包装耐热性，接头到环境， °C/W

$P_d = P_{Int} + P_{I/O}$

P_{Int}=我 女儿 ×v 女儿，瓦特——芯片内部电源

$P_{I/O}$=输入和输出引脚上的功耗——用户确定

对于大多数应用程序，$P_{I/O} << P_{Int}$可以被忽视。P 之间的近似关系 d和 T 第十个英文字母J（如果$P_{I/O}$被忽视）是：

$$P_d = K \div (T_{第十个英文字母\ J} + 273\ °C) \quad \textit{Eqn。3-2}$$

求解 方程 3-1 和 方程 3-2 对于 K 给出：

$$K = P_d \times (T_{罗马字母的第一个字母} + 273\ °C) + \Theta_{JA} \times (P_d)^2 \quad \textit{Eqn。3-3}$$

其中K 是与特定部分相关的常数。K 可以通过测量P 从方程 3 中确定d已知T 的（平衡） 罗马字母的第一个字母。使用K 的这个值，P 的值d和 T 第十个英文字母J可以通过求解获得 方程 3-1 和 方程 3-2 迭代的 T 的任何值 罗马字母的第一个字母·

3.5 ESD 保护和闩锁免疫

虽然静电放电（ESD）的损坏在这些设备上比在早期的 CMOS 电路上要少得多，但应采取正常的处理预防措施，以避免暴露于静电放电。进行资格测试，以确保这些设备能够承受合理水平的静电暴露，而不会受到任何永久性损坏。

所有 ESD 测试都符合汽车级集成电路的 AEC-Q100 应力测试资格。在设备认证期间，对人体模型（HBM）、机器模型（MM）和充电设备模型（CDM）进行了 ESD 应力。

如果暴露于 ESD 脉冲后，设备不再符合设备规范，则设备被定义为故障。除非设备规格另有指示，否则根据适用的设备规格在室温下进行完整的直流参数和功能测试，然后是高温。

表 6。ESD 和闩锁测试条件

型号	描述	标志	价值	单位
人体模型	系列电阻	R1	1500	Ω

	存储电容	字母 C	100	pF
	每个引脚的脉冲数	—	3	
费用装置型号	系列电阻	R1	0	Ω
	存储电容	字母 C	200	pF
	每个引脚的脉冲数	—	3	
锁定	最小输入电压限制		–2.5	v
	最大输入电压限制		7.5	v

表 7。ESD 和闩锁保护特性

不。	评分 [5]	标志	分钟	马克斯	单位
1	人体模型（HBM）	VHBM	±2000	—	v
2	充电设备型号（CDM）	VCDM	±500	—	v
3	T 的闩锁电流罗马字母的第一个字母= 85 °字母 C	我 LAT	±100	—	妈

3.6 DC 特性

本节包括有关电源要求和 I/O 引脚特性的信息。

表 8。DC 特性

全国矿工联盟	字母 C	特征	标志	状况	分钟	类型 [1]	马克斯	单位
1		工作电压			1.8		3.6	v
2	字母 C	输出高压 PTA[0:3]，PTA[6:7]，PTB[0:7]，PTC[0:7][2]，低驱动强度	v 啊	v 女儿>1.8 v I 供电量= –0.6 毫安	v 女儿– 0.5	—	—	v
	P	PTA[0:3]，PTA[6:7]，PTB[0:7]，PTC[0:7][2]，高驱动强度		v 女儿> 2.7 v I 供电量= –10 毫安	v 女儿– 0.5	—	—	
	字母 C			v 女儿> 1.8 v I 供电量= –3 毫安	v 女儿– 0.5	—	—	

[5] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3	字母C	输出高压	PTA[4:5]，PTD[0:7]，PTE[0:7]，低驱动强度	V 啊	V 女儿> 1.8 V I 供电量= –0.5 毫安	V 女儿– 0.5	—	—	V
	P		PTA[4:5]，PTD[0:7]，PTE[0:7]，高驱动强度		V 女儿> 2.7 V I 供电量= –3 毫安	V 女儿– 0.5	—	—	
	字母C				V 女儿> 1.8 V I 供电量= –1 毫安	V 女儿– 0.5	—	—	
4	d	输出大电流	最大总数 I 啊对于所有端口	我 OHT		—	—	100	妈
5	字母C	输出低电压	PTA[0:3]，PTA[6:7]，PTB[0:7]，PTC[0:7]，低驱动强度	VOL	V 女儿>1.8 V I 供电量= 0.6 毫安	—	—	0.5	V
	P		PTA[0:3]，PTA[6:7]，PTB[0:7]，PTC[0:7]，高驱动强度		V 女儿> 2.7 V I 供电量= 10 毫安	—	—	0.5	
	字母C				V 女儿> 1.8 V I 供电量= 3 毫安	—	—	0.5	
6	字母C	输出低电压	PTA[4:5]，PTD[0:7]，PTE[0:7]，低驱动强度	VOL	V 女儿> 1.8 V I 供电量= 0.5 毫安	—	—	0.5	V
	P		PTA[4:5]，PTD[0:7]，PTE[0:7]，高驱动强度		V 女儿> 2.7 V I 供电量= 3 毫安	—	—	0.5	
	字母C				V 女儿> 1.8 V I 供电量= 1 毫安	—	—	0.5	
7	d	输出低电流	最大总数 I_{OL} 对于所有端口	我 OLT		—	—	100	妈
8	P	输入高压	所有数字输入	VIH	V 女儿 >2.7 V	0.70 ×V 女儿	—	—	V
	字母C				V 女儿 > 1.8 伏	0.85 ×V 女儿	—	—	
9	P	输入低电压	所有数字输入	V_{IL}	V 女儿 >2.7 V	—	—	0.35 x V 女儿	
	字母C				V 女儿 > 1.8 伏	—	—	0.30 x V 女儿	
10	字母C	输入滞后	所有数字输入	V 歇斯		0.06 ×V 女儿	—	—	毫伏

表 8。直流特性（续）

全国矿工联盟	字母C	特征	标志	状况	分钟	类型[6]	马克斯	单位
11	P	输入泄漏电流 除 LCD 引脚（LCD 16-29）外，所有仅输入引脚	|我锢|	v 锢= V 女儿	—	0.025	1	M 罗马字母的第一个字母
				v 锢= V 纳粹党卫军	—	0.025	1	M 罗马字母的第一个字母
		仅 LCD 引脚（LCD 16-29）		v 锢= V 女儿	—	100	150	M 罗马字母的第一个字母
				v 锢= V 纳粹党卫军	—	0.025	1	M 罗马字母的第

[6] Typical values are measured at 25 °C. Characterized, not tested [2]

All I/O pins except for LCD pins in open drain mode.

								一个字母
12	P	Hi-Z（非状态）泄漏电流	所有输入/输出（每针）	|我盎司|	v 锢 = V 女儿 或 V 纳粹党卫军	—	0.025	1	M 罗马字母的第一个字母
13	P	总泄漏电流 [7][8][9] [10]	所有引脚的总泄漏电流	|我 InT|	v 锢 = V 女儿 或 V 纳粹党卫军	—	—	2	M 罗马字母的第一个字母
14	P	启用时上拉、下拉电阻	PTA[0:3]，PTA[6:7]，PTB[0:7]，PTC[0:7]	字母 RPU，字母 R 付讫	—	17.5	—	52.5	KΩ
	P		PTA[4:5]，PTD[0:7]，PTE[0:7]					69.5	
15	d	直流注入电流 [4]，[5]，[6]	单针限制	我 IC	v 锢 < V 纳粹党卫军，V 锢 > V 女儿	–0.2	—	0.2	妈
			总 MCU 限制，包括所有重压引脚的总和			–5	—	5	妈

[7] Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

[8] All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD}.

[9] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

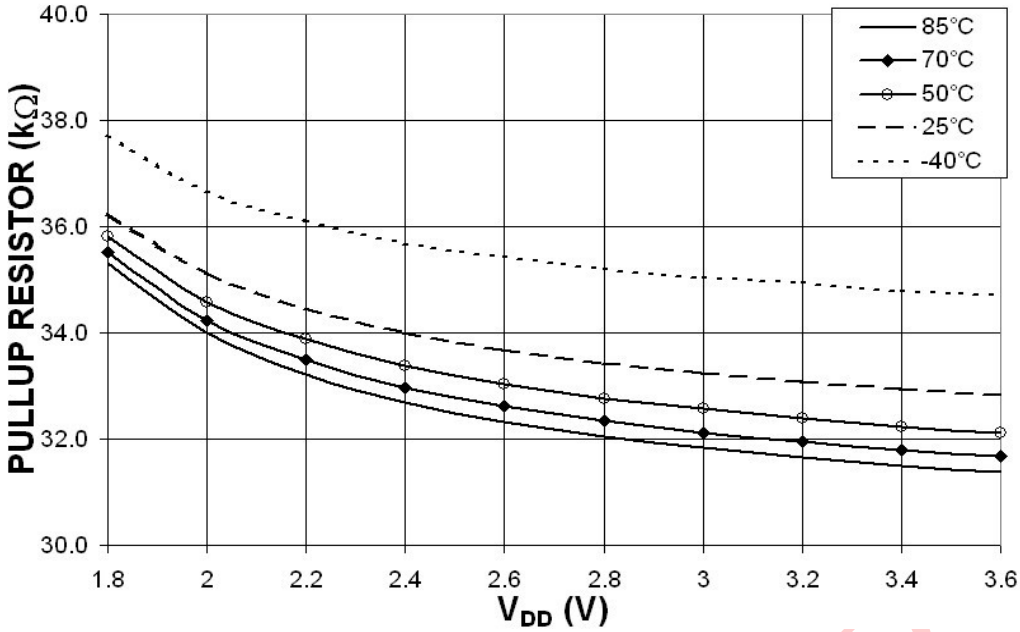
[10] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

16	字母 C	输入电容，所有引脚	字母 C 锢		—	—	8	pF
17	字母 C	RAM 保留电压	v 公羊		—	0.6	1.0	v
18	字母 C	POR 重新武装电压 [11]	VPOR		0.9	1.4	2.0	v
19	d	POR 重新武装时间	字母 TPOR		10	—	—	M 罗马字母的第十九个
20	P	低压检测阈值	VLVD	v 女儿下降 V 女儿上升	1.80 1.88	1.84 1.92	1.88 1.96	v
21	P	低压警告阈值	VLVW	v 女儿下降 V 女儿上升	2.08	2.14	2.2	v
22	P	低压抑制复位/恢复滞后	v 歇斯		—	80	—	毫伏
23	P	带隙电压参考 [12]	VBG		1.15	1.17	1.18	v

[11] POR will occur below the minimum voltage.

[12] Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C.

PULLUP RESISTOR TYPICALS - Non LCD Pins



PULLDOWN RESISTOR TYPICALS - Non LCD Pins

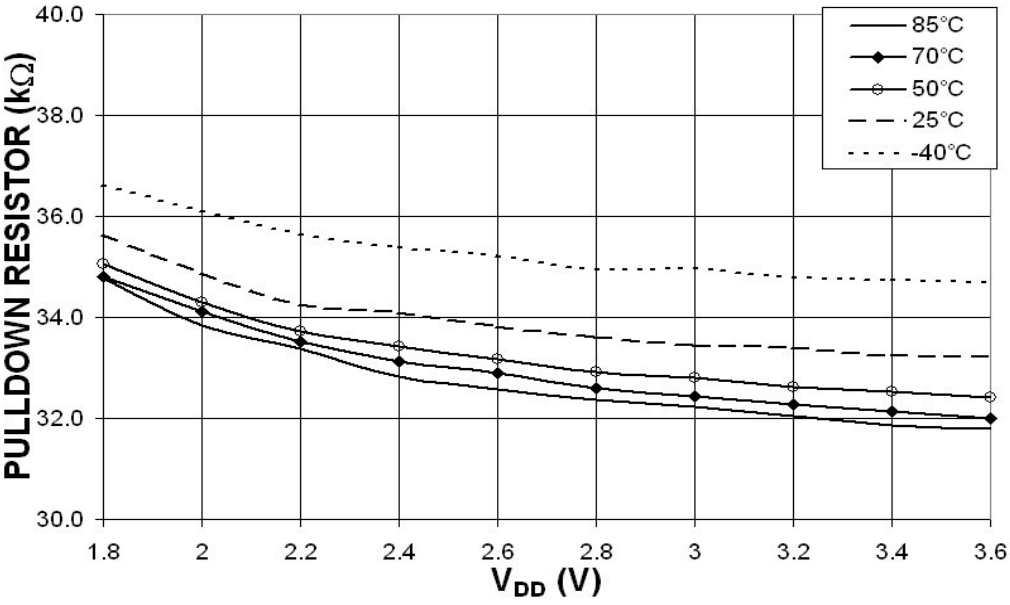


图 4。非 LCD 引脚 I/O 上拉和下拉典型电阻值（$V_{女儿}$= 3.0 V）

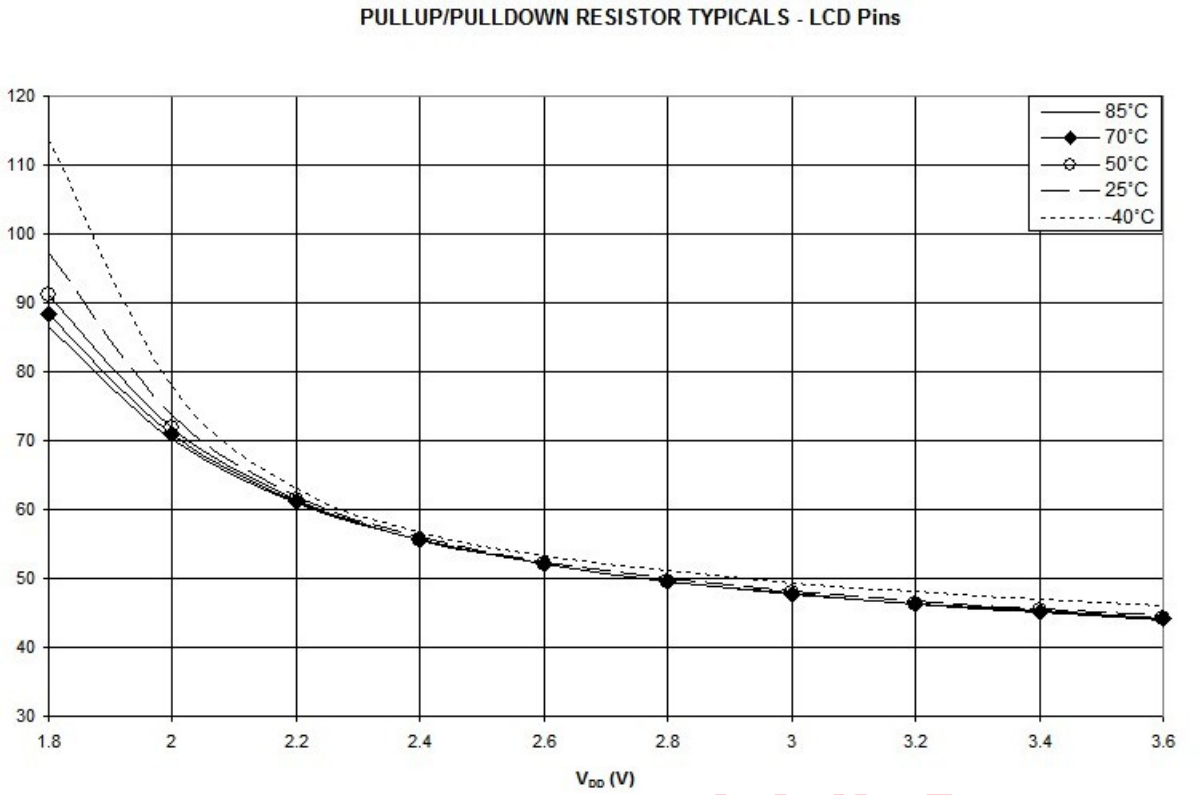
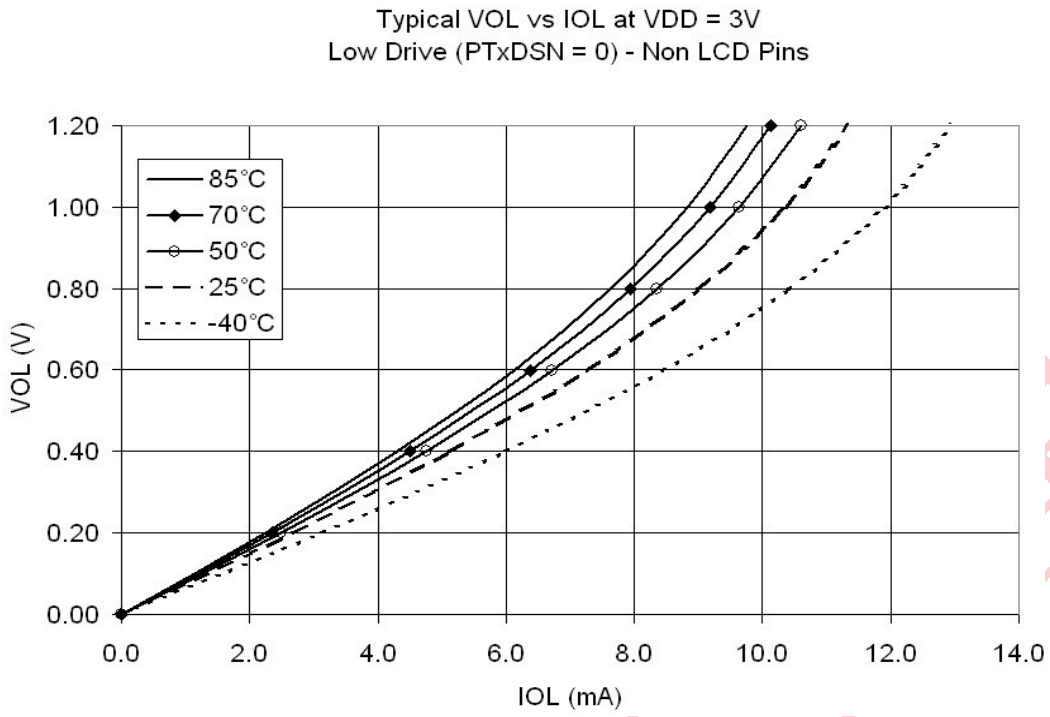


图 5。LCD/GPIO 引脚 I/O 上拉/下拉典型电阻值



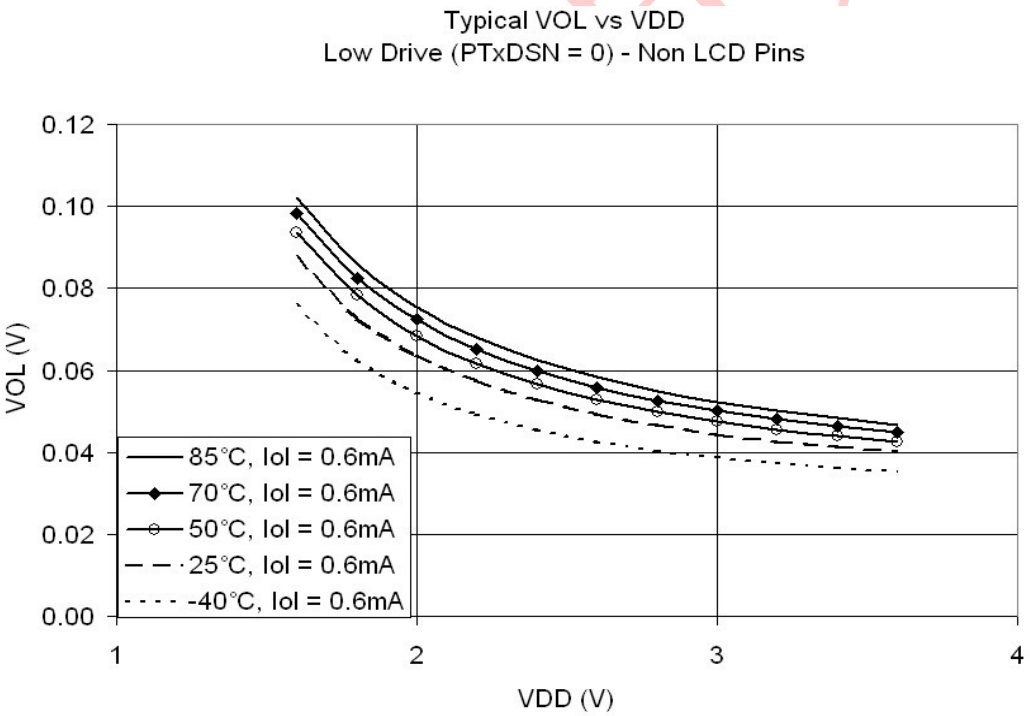
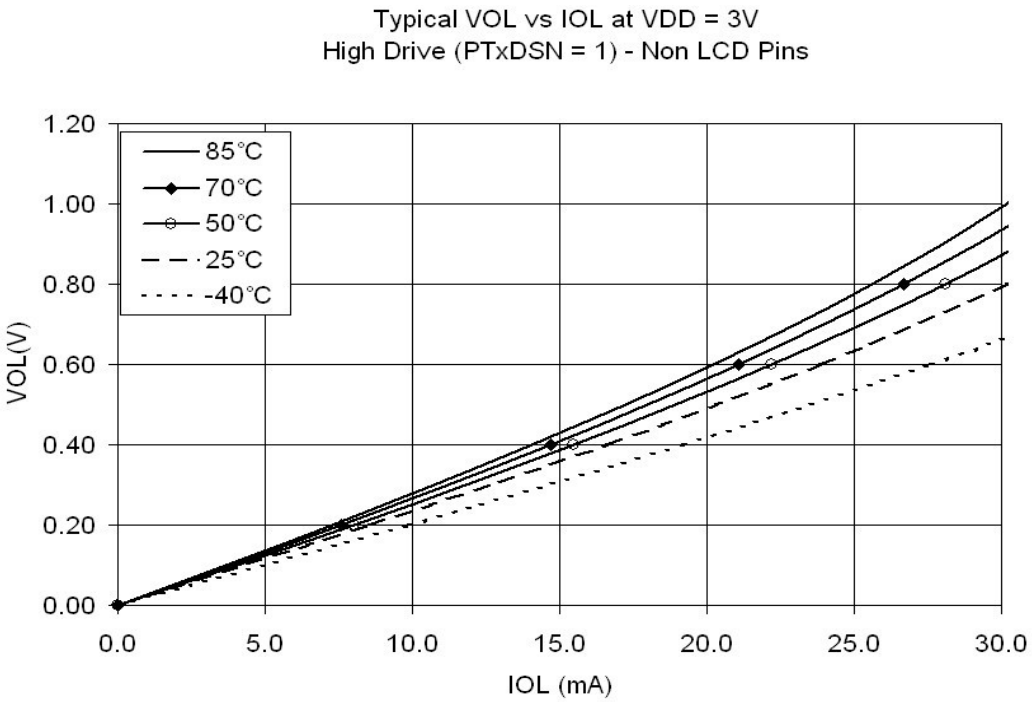


图 6。典型的低侧驱动器（水槽）特性（非 LCD 引脚）—低驱动（PTxDSn = 0）



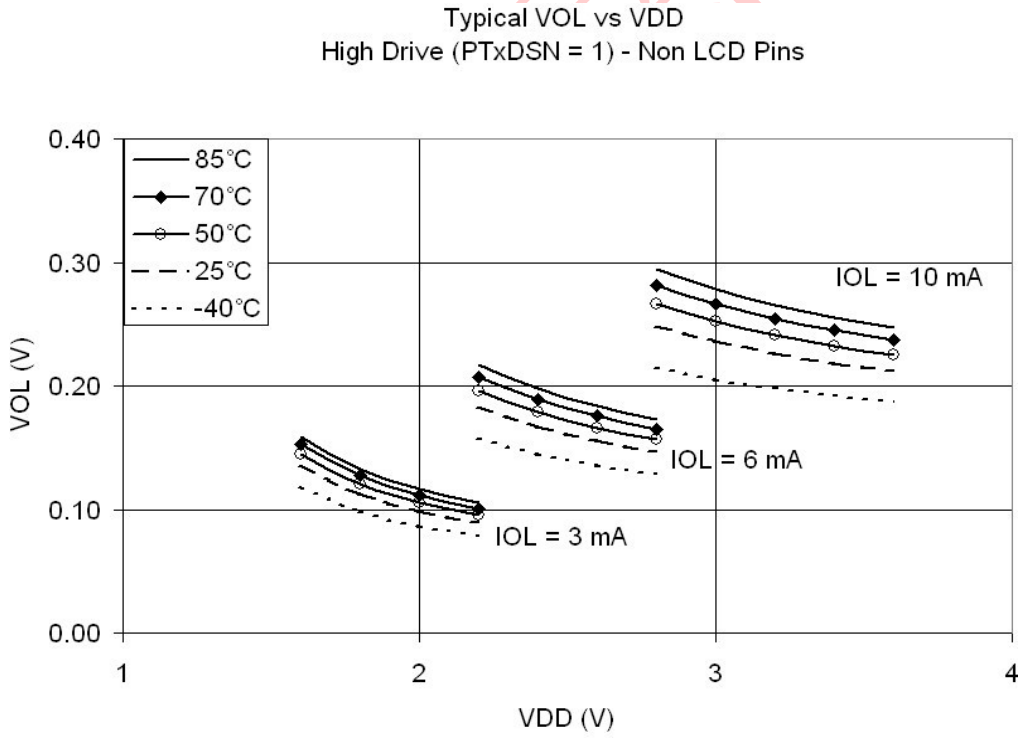


图 7。典型的低侧驱动器（水槽）特性（非 LCD 引脚）— 高驱动（PTxDSn = 1）

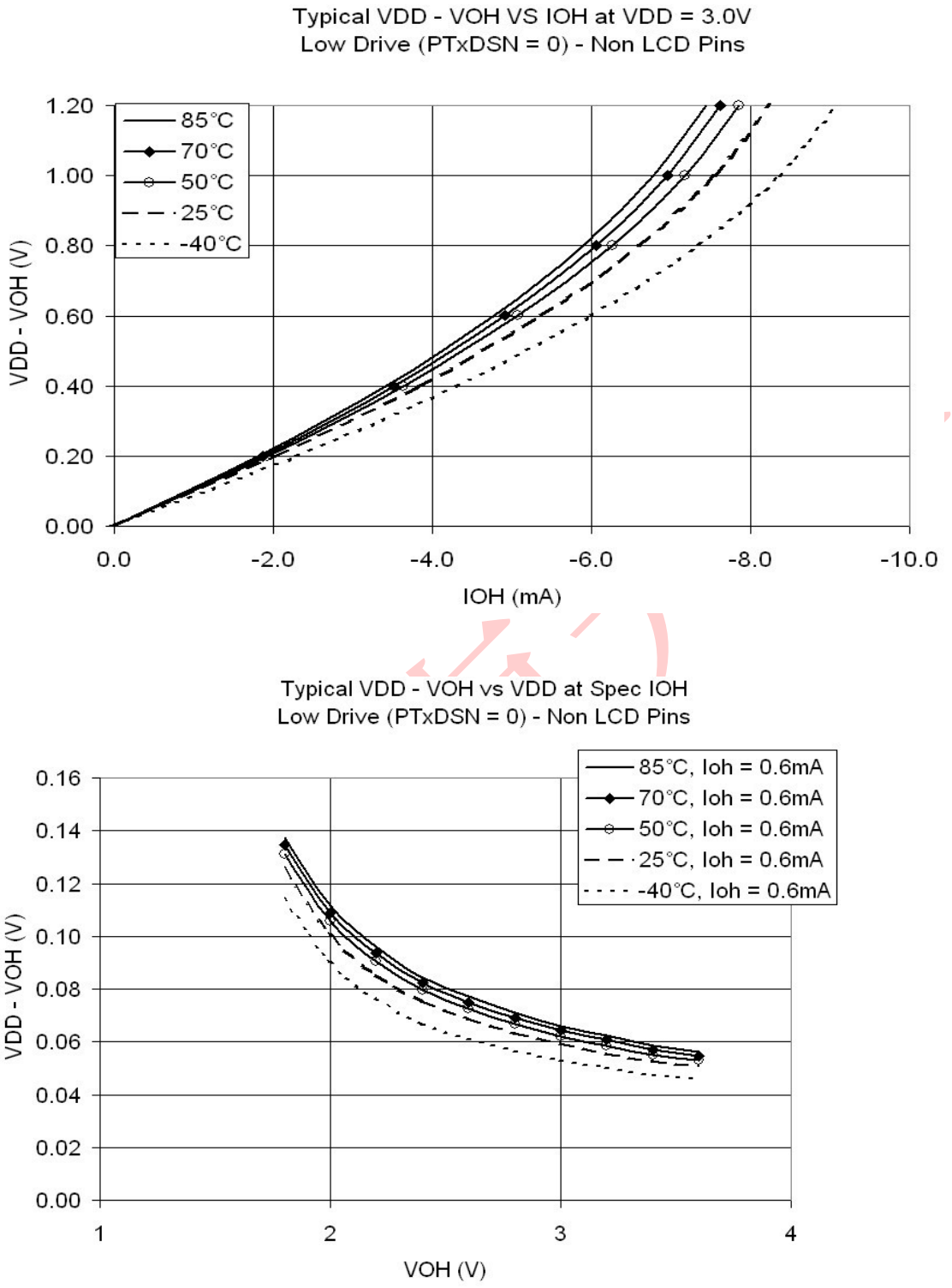


Figure 8. Typical High-Side (Source) Characteristics (Non-LCD Pins) — Low Drive (PTxDSn = 0)

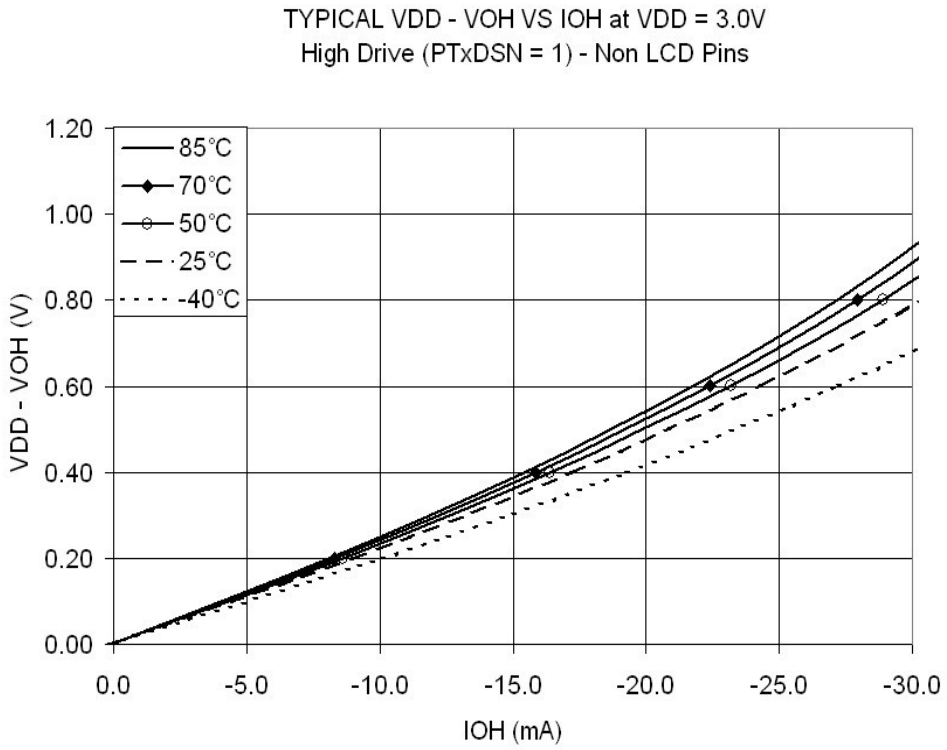
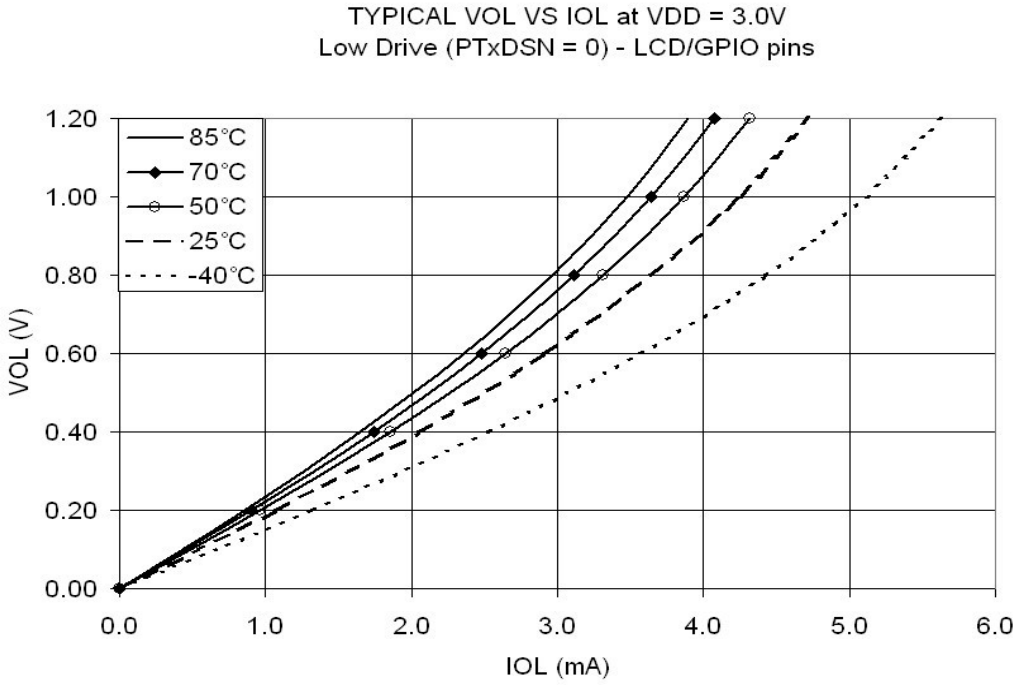


Figure 9. Typical High-Side (Source) Characteristics(Non-LCD Pins) — High Drive (PTxDSn = 1)



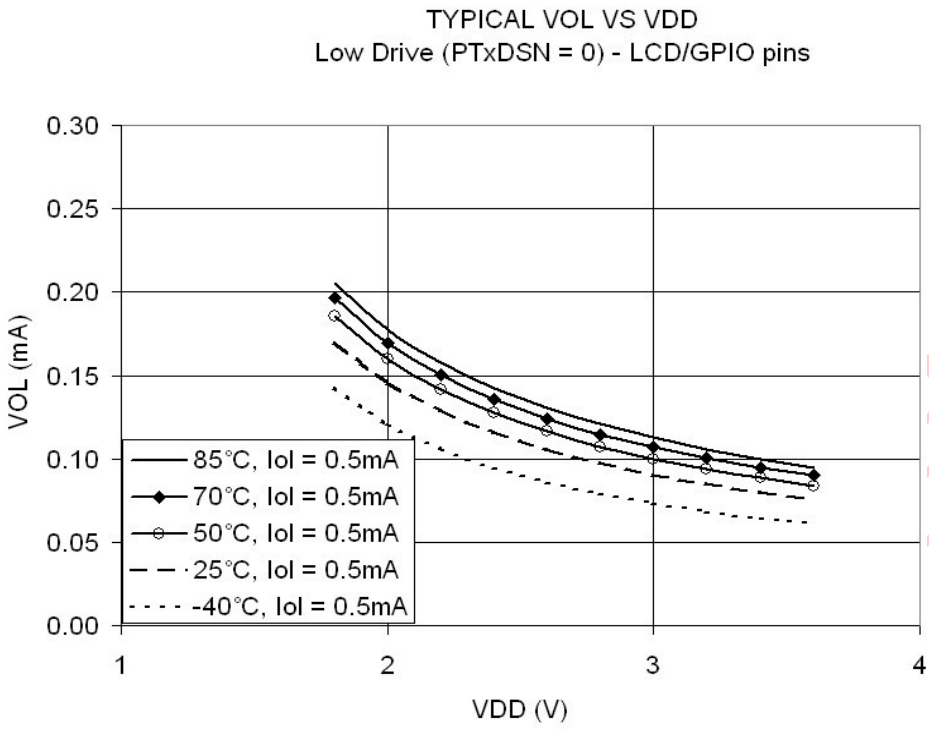
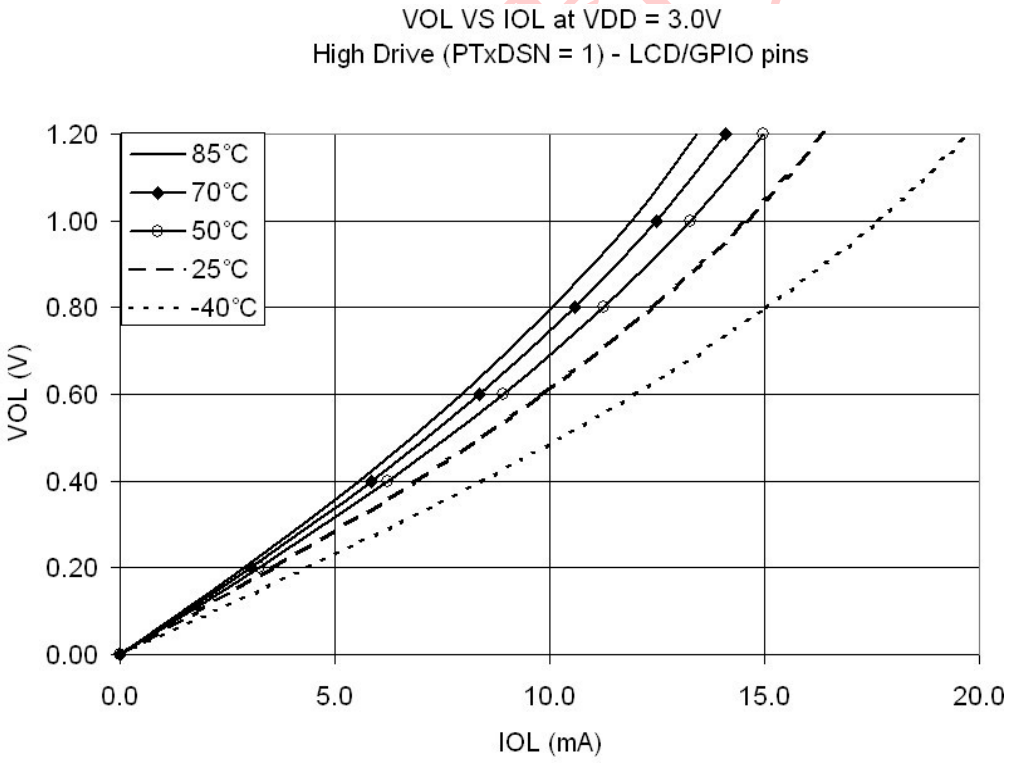


Figure 10. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO Pins) — Low Drive (PTxDSn = 0)



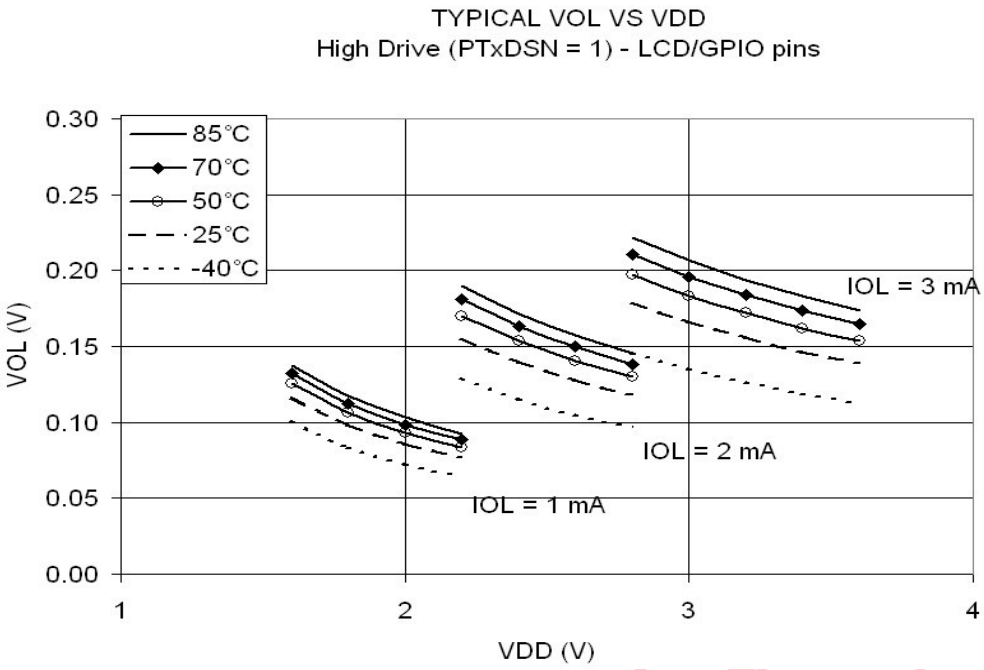
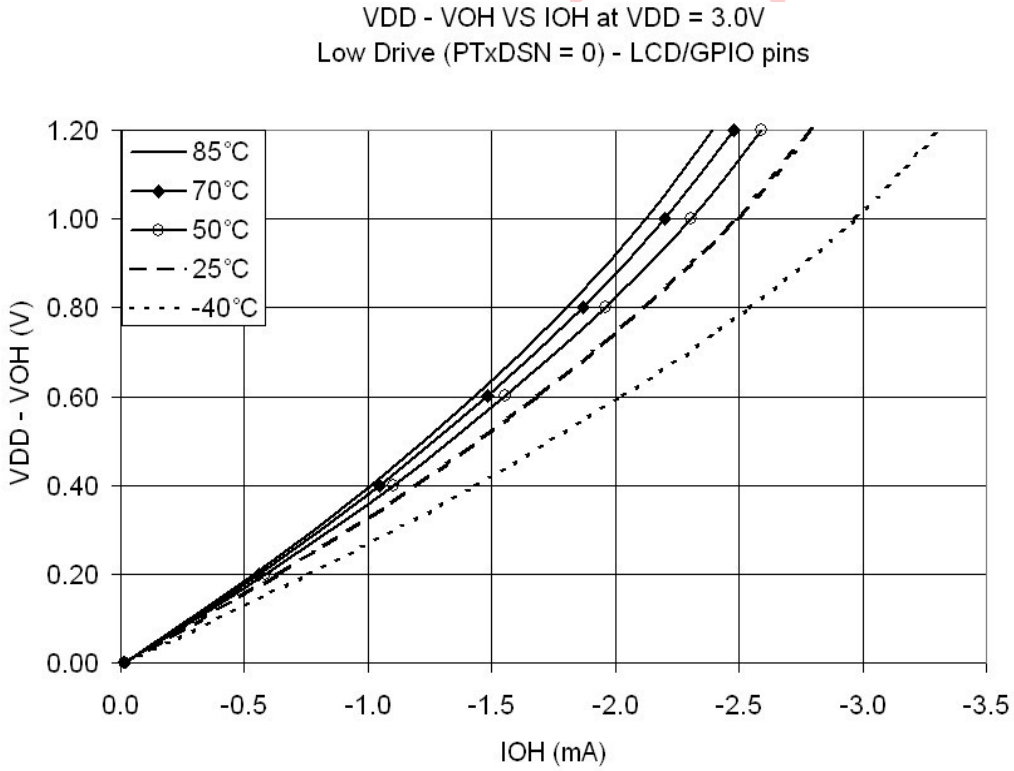


Figure 11. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO Pins) — High Drive (PTxDSn = 1)



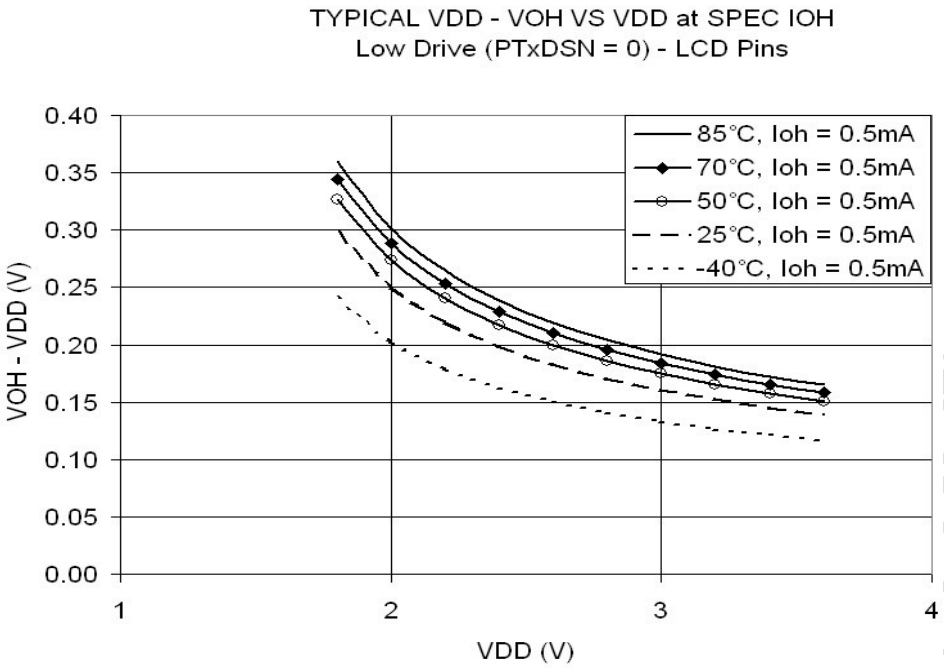
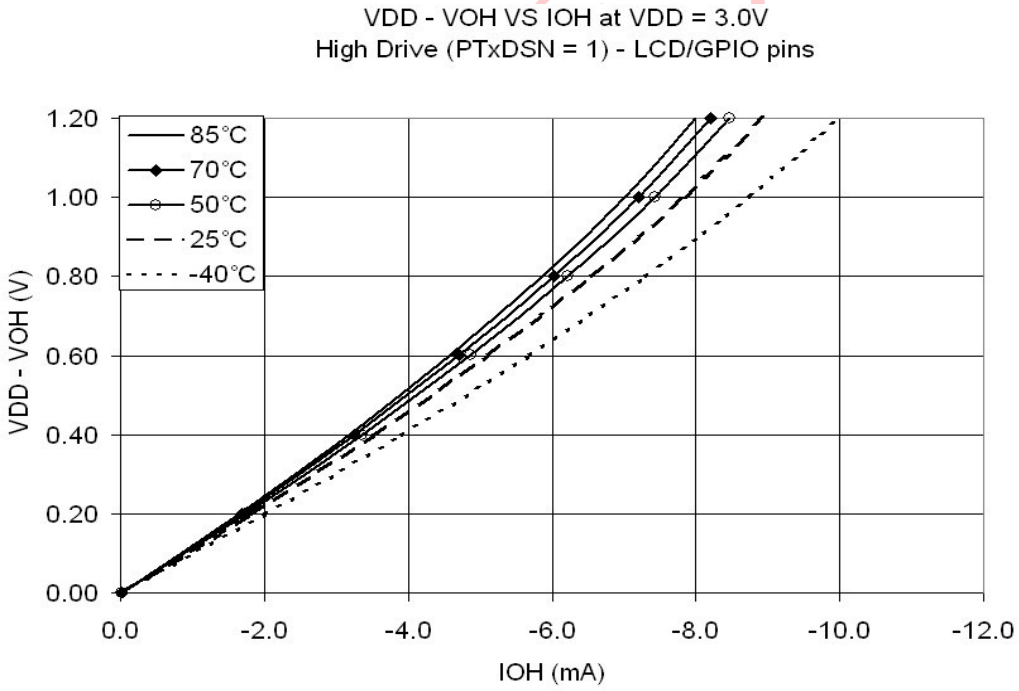


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO Pins) — Low Drive (PTxDSn = 0)



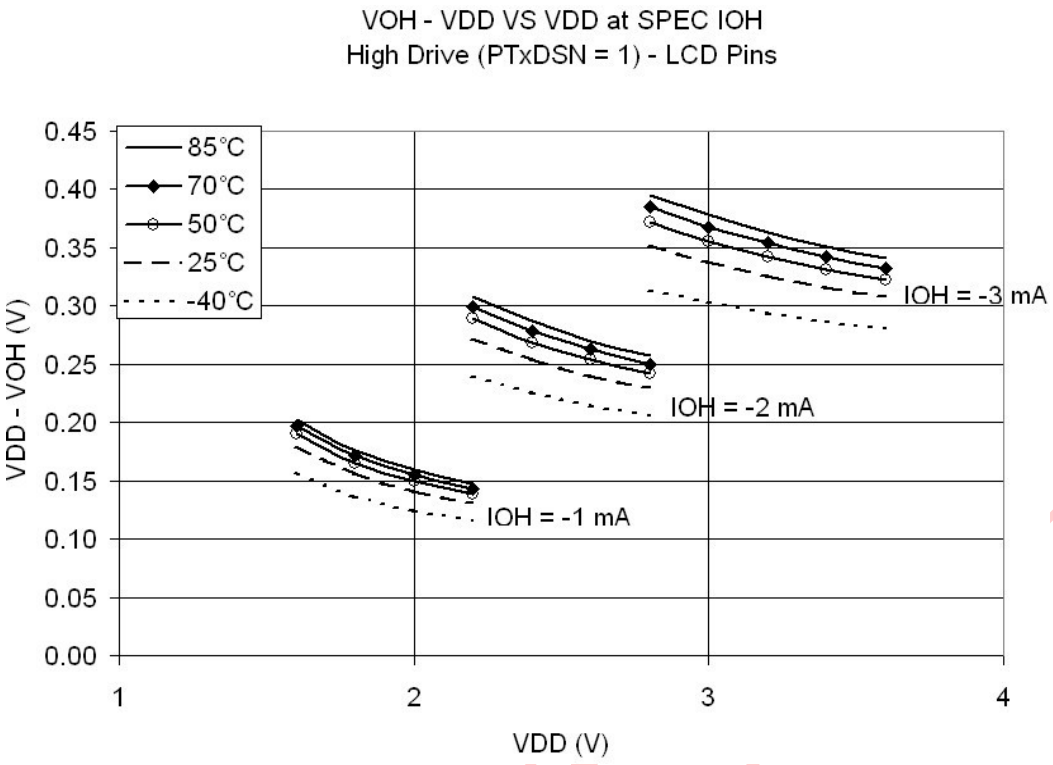


Figure 13. Typical High-Side (Source) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	R_{IDD}	8 MHz	3	4.2	5.7	mA	–40 to 85 °C
	T			1 MHz		1	1.52		
2	T	Run supply current FEI mode, all modules off	R_{IDD}	10 MHz	3	3.60	—	mA	–40 to 85 °C
	T			1 MHz		0.50	—		
3	T	Run supply current LPRS=0, all modules off	R_{IDD}	16 kHz FBILP	3	165	—	µA	–40 to 85 °C
	T			16 kHz FBELP		105	—		
4	T	Run supply current	R_{IDD}	16 kHz FBILP	3	77	—	µA	–40 to 85 °C

	T	LPRS=1, all modules off; running from Flash		16 kHz FBELP		21	—		
5	T	Run supply current LPRS=1, all modules off; running from RAM	RI_{DD}	16 kHz FBILP	3	77	—	µA	–40 to 85 °C
	T			16 kHz FBELP		7.3	—		
6	P	Wait mode supply current FEI mode, all modules off	WI_{DD}	8 MHz	3	1.4	3.5	mA	–40 to 85 °C
	C			1 MHz		0.8	1.15		
7	T	Wait mode supply current LPRS = 1, all modules off	WI_{DD}	16 kHz FBELP	3	1.3	—	µA	–40 to 85 °C
8	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	350	930	nA	–40 to 25 °C
						1000	—		50 °C
						2500	4000		70 °C
						5100	—		85 °C
	C			n/a	2	250	—		–40 to 25 °C
						2000	—		70 °C
						4000	—		85 °C
9	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	400	1030	nA	–40 to 25 °C
						1300	—		50 °C
						4000	6000		70 °C
						8000	—		85 °C
	C			n/a	2	350	—		–40 to 25 °C
						3000	—		70 °C
						6000	—		85 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
10	C	Application Stop3 mode supply current[2]	$ApS3I_{DD}$	n/a	3	6.1	—	µA	25 °C
11	C	Application Stop3 mode supply current[2]	$ApS3I_{DD}$	n/a	3	7.5	—	µA	50 °C

1 Typical values are measured at 25 °C. Characterized, not tested.

2 32 kHz crystal enabled in low power mode. TOD module enabled. V_{IREG} enabled for 3 V LCD glass 500pf 8x24 LCD glass at
32 Hz frame rate with LCD Charge pump clock set to low setting and every other segment “on.”

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				–40	25	70	85	
1	T	LPO		100	100	150	175	nA
2	T	ERREFSTEN	RANGE = HGO = 0	250	360	400	460	nA
3	T	IREFSTEN[1]		63	70	77	81	µA
4	T	TOD	Does not include clock source current	50	50	75	100	nA
5	T	LVD[1]	LVDSE = 1	110	110	112	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	12	12	20	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	95	101	120	µA
8	T	LCD	VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 Segments, 32Hz frame rate, No LCD glass connected.	1	1	4.2	12	µA

3.8 External Oscillator (XOSCVLP) Characteristics

Refer to Figure 14 and Figure 15 for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[2]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz

1 Not available in stop2 mode.

2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note [1] See Note [2]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	— — —	— 10 1	— — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	— 100 0 0 0 0	— — — 0 10 20	kΩ
5	C	Crystal start-up time [3] Low range, low power Low range, high gain High range, low power High range, high gain	t_{CSTL} t_{CSTH}	— — — —	600 400 5 15	— — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	0.03125 0	— —	20 20	MHz MHz

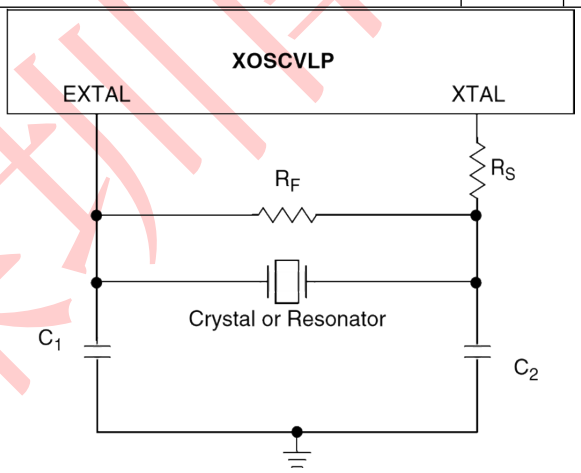


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

[1] Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

[2] See crystal or resonator manufacturer's recommendation.

[3] Proper PC board layout procedures must be followed to achieve specifications.

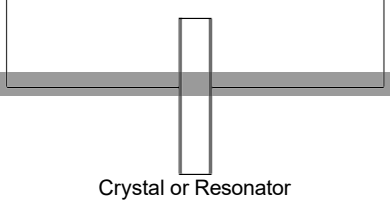


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - trimmed	f_{int_t}	31.25	—	39.063	kHz
3	T	Internal reference start-up time	t_{IRST}	—	—	6	µs
4	P	DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16.8	21.33	MHz
5	P	DCO output frequency range - trimmed	f_{dco_t}	16	—	20	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta^{f}_{dco\_res\_t}$	—	±0.1	±0.2	%f_{dco}
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta^{f}_{dco\_res\_t}$	—	±0.2	±0.4	%f_{dco}
8	C	Total deviation from trimmed DCO output frequency over voltage and temperature	$\Delta^{f}_{dco\_t}$	—	+ 0.5 – 1.0	±2	%f_{dco}

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
9	C	Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	$\Delta^{f}_{dco\_t}$	—	±0.5	±1	%f_{dco}
10	C	FLL acquisition time [2]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [3]	C_{Jitter}	—	0.02	0.2	%f_{dco}

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

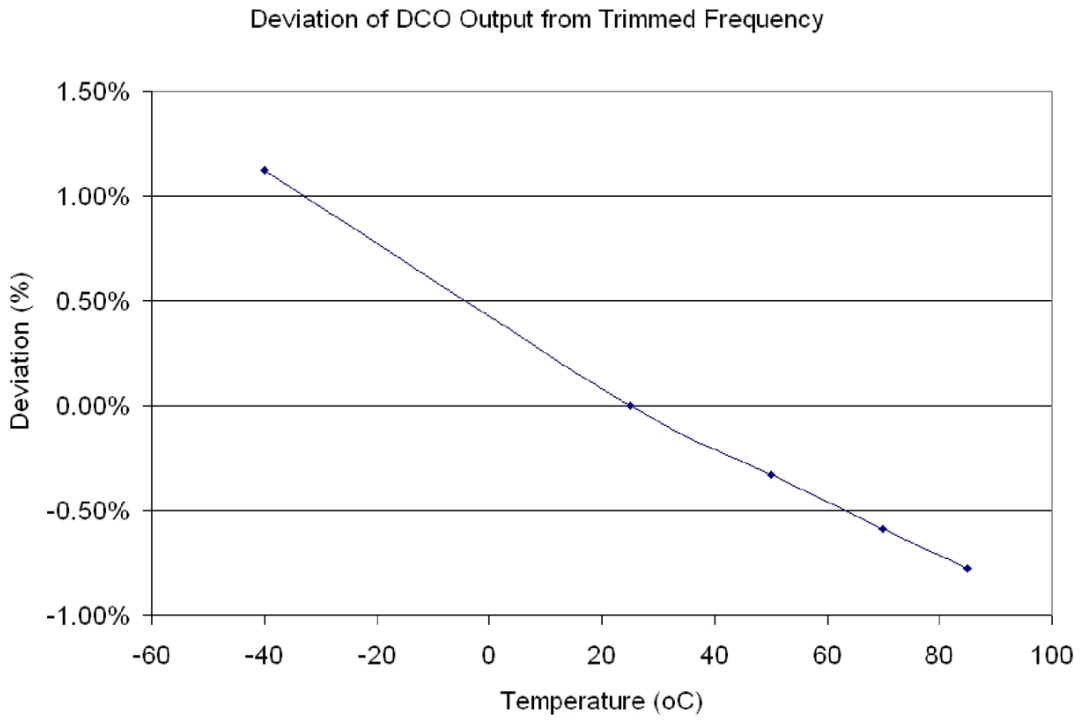


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 × t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 × t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 × t_{cyc}	— —	— —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage Regulator Recovery time	t_{VRR}	—	6	10	us

[1] Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

[3] To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

[4] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

[5] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

[6] Except for LCD pins in Open Drain mode.

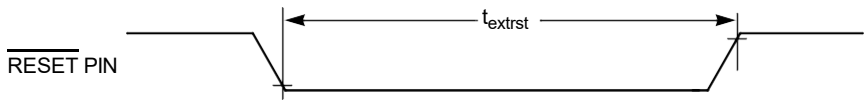


Figure 17. Reset Timing

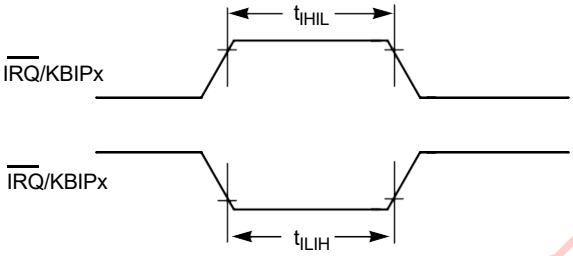


Figure 18. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TP Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	fTCLK	0	fBus/4	Hz
2	D	External clock period	tTCLK	4	—	tcyc
3	D	External clock high time	tclkh	1.5	—	tcyc
4	D	External clock low time	tclkl	1.5	—	tcyc
5	D	Input capture pulse width	tICPW	1.5	—	tcyc

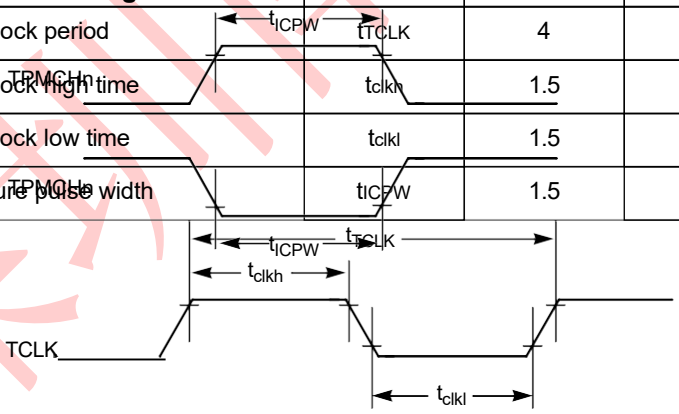


Figure 19. Timer External Clock

Figure 20. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 15 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

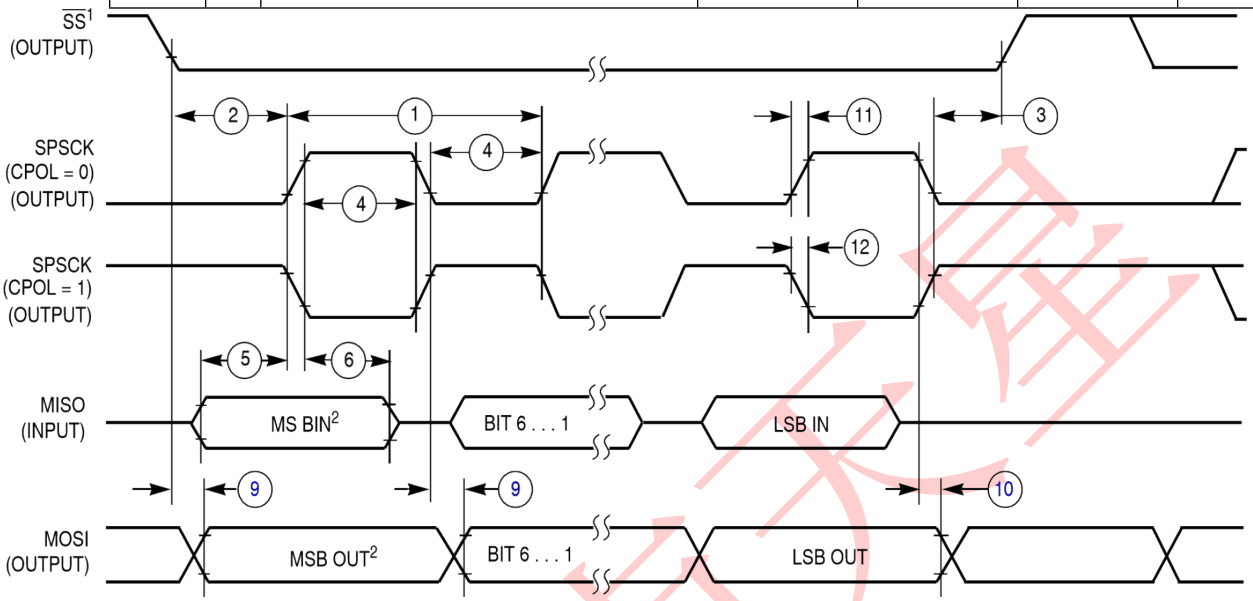
Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	t_{cyc} – 30 t_{cyc} – 30	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns

Table 15. SPI Timing (continued)

No.	C	Function	Symbol	Min	Max	Unit
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns

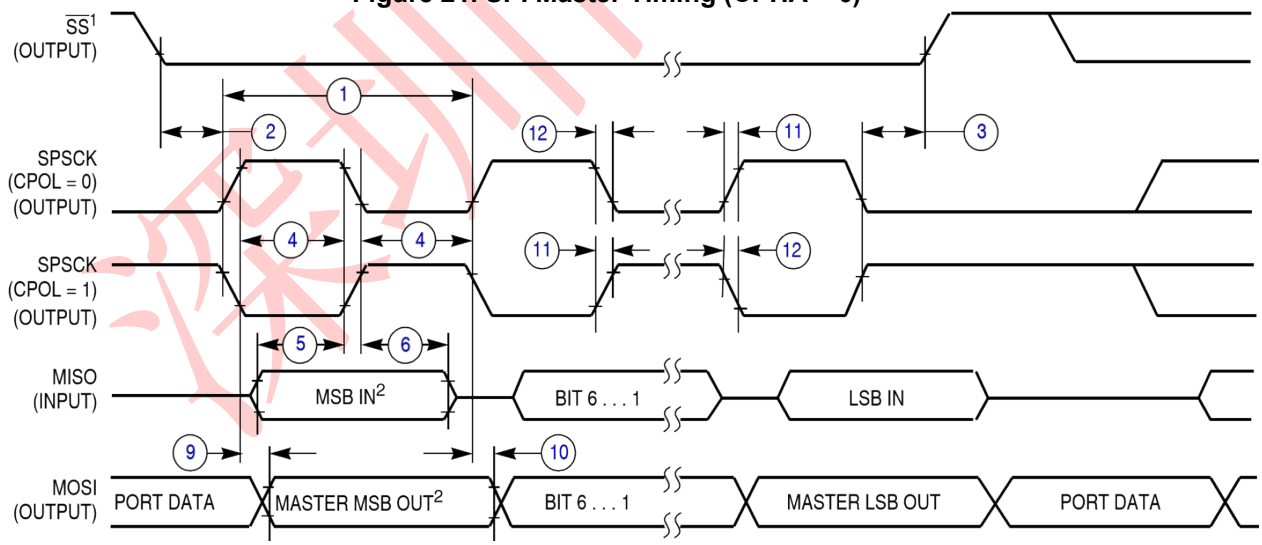
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	t_{cyc} – 25 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	t_{cyc} – 25 25	ns ns



NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. SPI Master Timing (CPHA = 0)

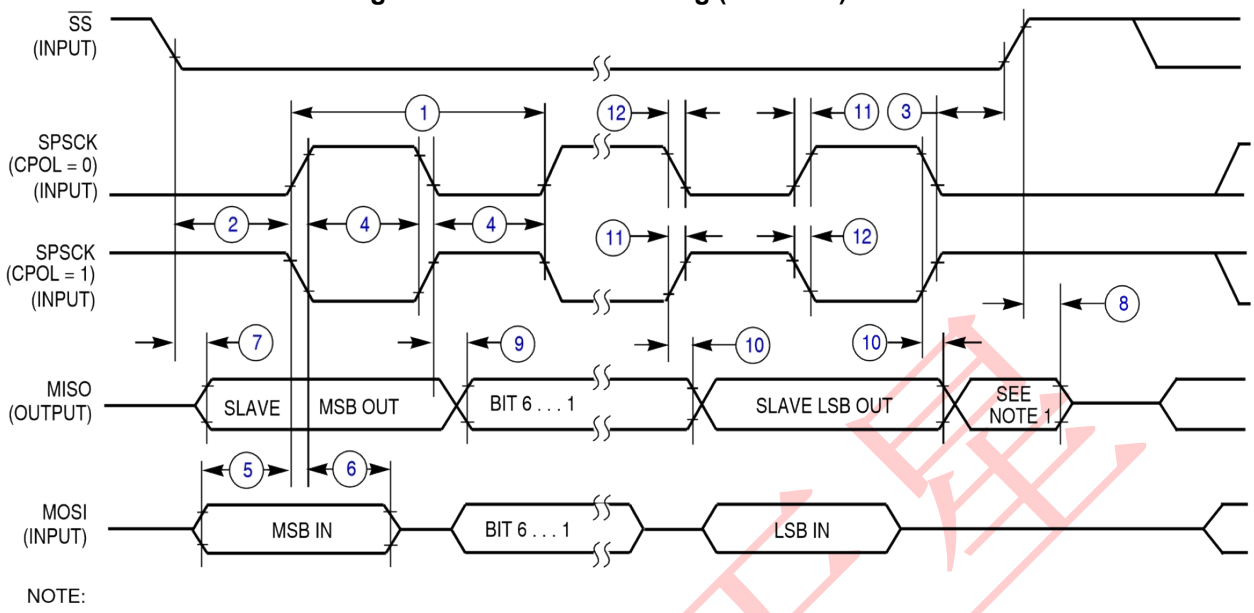


NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

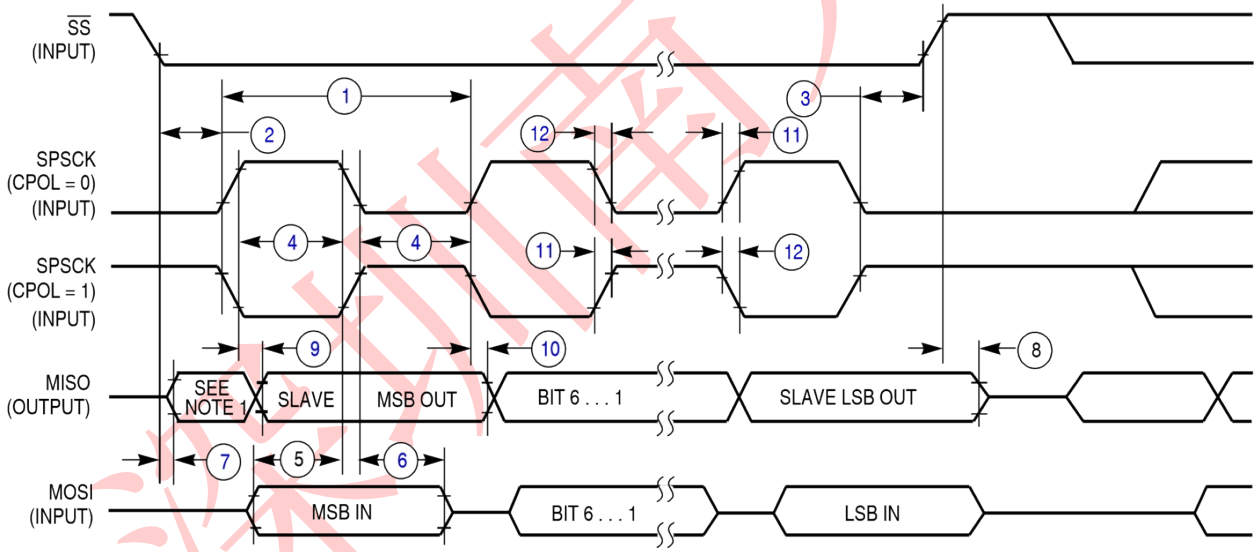
Figure 22. SPI Master Timing (CPHA =1)



NOTE:

1. Not defined but normally MSB of character just received. **Figure 23.**

SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received.

Figure 24. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
C	Supply current (active)	I_{DDAC}	—	20	35	µA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}		20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

3.12 ADC Characteristics

Table 17. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	1.8	—	3.6	V	
	Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	

Table 17. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Ref Voltage High		V_{REFH}	1.8	V_{DDA}	V_{DDA}	V	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	5	7	kΩ	
Analog Source Resistance	12-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		— —	— —	5 10		

	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

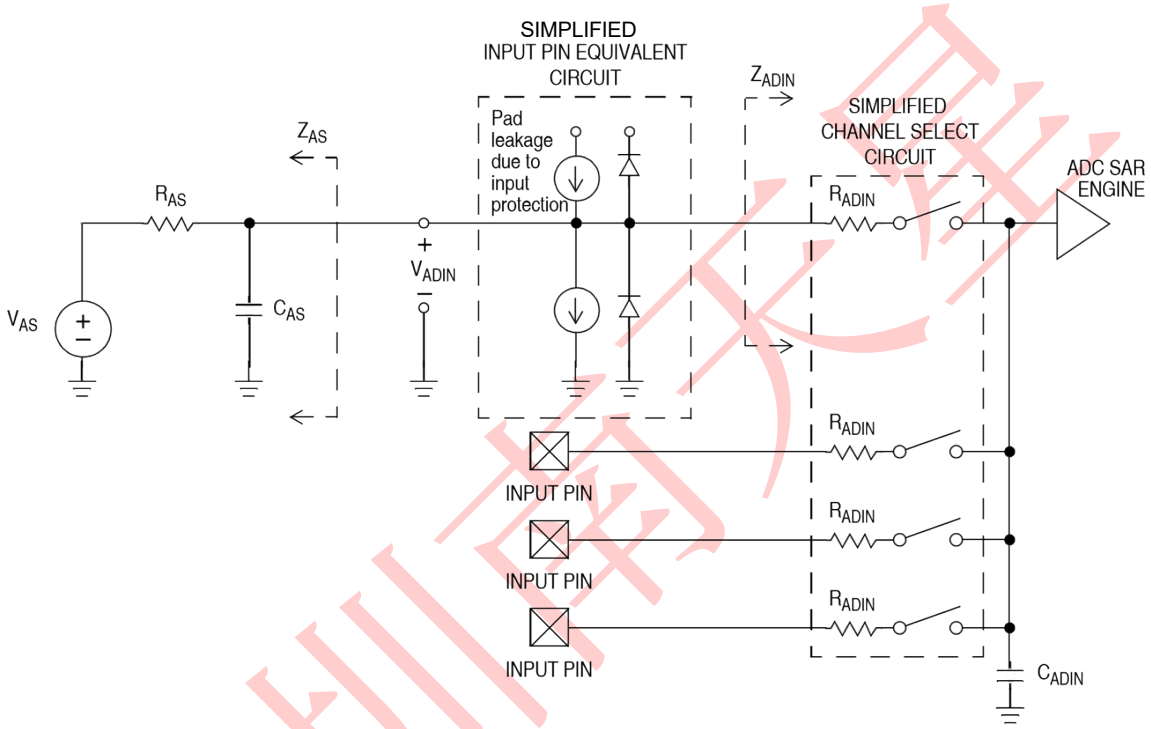


Figure 25. ADC Input Impedance Equivalency Diagram

Table 18. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Supply Current ADLPC=1 ADLSMP=1 ADCO=1		I_{DDA}	—	120	—	µA	
T	Supply Current ADLPC=1 ADLSMP=0 ADCO=1		I_{DDA}	—	200	—	µA	

T	Supply Current ADLPC=0 ADLSMP=1 ADCO=1		I_{DDA}	—	290	—	µA	
P	Supply Current ADLPC=0 ADLSMP=0 ADCO=1		I_{DDA}	—	0.53	1	mA	
P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
C		Low Power (ADLPC=1)		1.25	2	3.3		
P	Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See ADC chapter in the LL16 Reference Manual for conversion time variances
C		Long Sample (ADLSMP=1)		—	40	—		
P	Sample Time	Short Sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
C		Long Sample (ADLSMP=1)		—	23.5	—		
T	Total Unadjusted Error	12-bit mode, 3.6>VDDA>2.7V	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
		12-bit mode, 2.7>VDDA>1.8V		—	–1 to 3	–3.0 to 6.0		
P		10-bit mode		—	±1	±2.5		
T		8-bit mode		—	±0.5	±1.0		
T	Differential Non-Linearity	12-bit mode	DNL	—	±1	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
T		8-bit mode[3]		—	±0.3	±0.5		
T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	–2.5 to 1.0	LSB[2]	
P		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		

Table 18. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
T	Zero-Scale Error	12-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	$V_{ADIN} = V_{SSA}$
P		10-bit mode		—	±0.5	±1.5		
T		8-bit mode		—	±0.5	±0.5		

T	Full-Scale Error	12-bit mode	E_{FS}	—	±1	–3.5 to 1.0	LSB[2]	$V_{ADIN} = V_{DDA}$
P		10-bit mode		—	±0.5	±1		
T		8-bit mode		—	±0.5	±0.5		
D	Quantization Error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		
D	Input Leakage Error	12-bit mode	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		
D	Temp Sensor Slope	–40 °C to 25 °C	m	—	1.646	—	mV/°C	
		25 °C to 85 °C		—	1.769	—		
D	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	

[1] Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = (V_{REFH} – V_{REFL})/2N

[3] Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes [4] Based on input pad leakage current. Refer to pad electricals.

3.13 LCD Specifications

Table 19. LCD Electricals, 3 V Glass

C	Characteristic		Symbol	Min	Typ	Max	Unit
D	LCD Supply Voltage		V_{LCD}	0.9	1.5	1.8	V
D	LCD Frame Frequency		fFrame	28	30	58	Hz
D	LCD Charge Pump Capacitance		C_{LCD}		100	100	nF
D	LCD Bypass Capacitance		C_{BYLCD}		100	100	nF
D	LCD Glass Capacitance		Cglass		2000	8000	pF
D	V_{IREG}	HRefSel = 0 HRefSel = 1	V_{IREG}	.89 1.49	1.00 1.67	1.15 1.85[1]	V
D	V_{IREG} TRIM Resolution		ΔR_{TRIM}	1.5			% V_{IREG}
D	V_{IREG} Ripple	HRefSel = 0 HRefSel = 1				0.1 0.15	V

D	V_{LCD} Buffered Adder[2]	IBuff		1		µA

1 V_{IREG} Max can not exceed V_{DD} – 0.15 V

2 VSUPPLY = 10, BYPASS = 0

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.
For more detailed information about program/erase operations, see the Memory section.

Table 20. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{prog/erase}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
P	Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}
P	Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
P	Page erase time[2]	t_{Page}		4000		t_{Fcyc}
P	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
D	Byte program current[3]	RI_{DDBP}	—	4	—	mA
D	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 Typical endurance for FLASH was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

3.15 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.15.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 21. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 3.3 V T_A = 25 °C package type 64-pin LQFP	0.15 – 50 MHz	32 kHz crystal 10 MHz bus	–7	dBµV
			50 – 150 MHz		–9	
			150 – 500 MHz		–6	
			500 – 1000 MHz		–6	
			IEC Level		N	—
			SAE Level		1	—

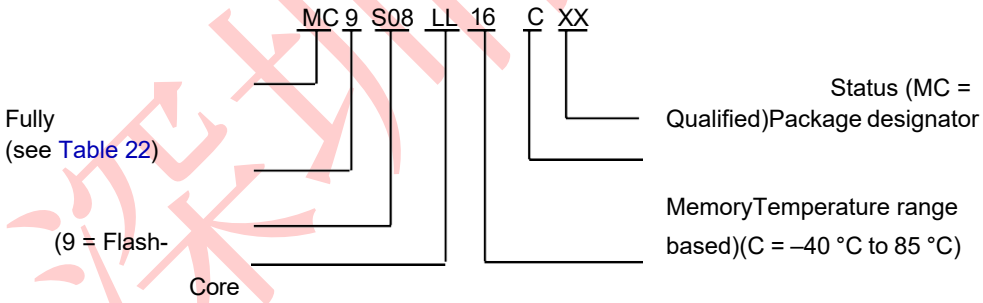
[1] Data based on qualification test results.

4 Ordering Information

This section contains the ordering information and the device numbering system for the MC9S08LL16 Series.

4.1 Device Numbering System

Example of the device numbering system:



Information and Mechanical Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08LL16 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 22) in the "Enter Keyword" search box at the top of the page.

Package Information and Mechanical Drawings

Table 22. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A
48	Quad Flat No-Leads	QFN	GT	1314	98ARH99048A

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